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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,915	02/22/2002	Fernando Gonzalez	MCRO:125--4/FLE 94-0281.0	4617

7590 09/22/2005

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EXAMINER	
PERALTA, GINETTE	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

N/A

Office Action Summary	Application No.	Applicant(s)	
	10/081,915	GONZALEZ ET AL.	
	Examiner	Art Unit	
	Ginette Peralta	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-60* is/are pending in the application.

4a) Of the above claim(s) *18,21-34,37-39 and 50-52* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19,20,35,36,40-49 and 53-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. In view of the arguments presented on the Appeal Brief filed on 6/9/05, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

ANH D. MAI
PRIMARY EXAMINER

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 19, 35, and 40-45 are rejected under 35 U.S.C. 102(b) as being anticipated by Ovshinsky et al. (U. S. Pat. 5,296,716).

Regarding claim 19, Ovshinsky discloses a method for making a memory device as the one shown in Fig. 2, the method comprising the steps of providing a substrate 10 having a first conductive line 12 therein; forming a plurality of memory cells 30, each memory cell comprising an element programmable to multiple states of resistance (as disclosed in co. 8, lines 4-10, and col. 12, lines 6-44; forming a second conductive line 42, the second conductive line 42 in electrical communication with one of the memory cells 30; and creating a third conductive line 29 in electrical communication with the first conductive line 12 and the plurality of memory cells 30.

Regarding claim 35, Ovshinsky discloses that the method further comprises forming a plurality of contacts 14 between the first conductive line 12 and the third conductive line 29, a respective one of the plurality of contacts being formed between respective pairs of memory cells 30.

Regarding claim 40, Ovshinsky discloses forming each of the memory cells to have a width approximately equal to a minimum photolithographic limit as disclosed in col. 12,lines 36-44.

Regarding claim 41, Ovshinsky discloses in col. 14, lines 13-20 that the forming of the memory cells, each pair being spaced apart by a distance that is limited only by the resolution of the lithography.

Regarding claim 42, Ovshinsky discloses in col. 11, lines 47-53 that each contact 14 is formed from a doped semiconductive region of the substrate.

Regarding claim 43, Ovshinsky discloses that the step of forming a plurality of contacts comprises forming dielectric spacers 16 between each pair of memory cells; and forming each contact 14 between the respective dielectric spacers 16.

Regarding claim 44, Ovshinsky discloses in col. 14, lines 13-20 that the forming of the structure, including each contact and its respective dielectric spacers have a combined width that is limited only by the resolution of the lithography.

Regarding claim 45, Ovshinsky discloses isolating each of the plurality of memory cells 30 from the plurality of contacts 14.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 20, 48, and 53-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Becker (U. S. Pat. 5,770,498) in view of Ovshinsky (U. S. Pat. 5,296,716) and Gonzalez et al. (U. S. Pat. 5,150,276).

Regarding claim 20, Becker discloses a method for making a memory array that comprises forming a digit line 28 in a substrate; forming a plurality of memory cells in a first insulative layer 36, the memory cells overlying the digit line 28 and in electrical communication with the digit line 28, the first insulative layer 36 having an opening therein; forming a contact plug 54 in the opening, the plug in electrical communication with the digit line 28; and forming a second conductive line 56 in a conductive layer, the second conductive line 56 in electrical communication with the contact plug.

Becker discloses the claimed invention with the exception of forming the memory cells comprising an element programmable to multiple states of resistance.

Ovshinsky discloses a method for making a memory device as the one shown in Fig. 2, the method comprising the steps of providing a substrate 10 having a first conductive line 12 therein; forming a plurality of memory cells 30, each memory cell comprising an element programmable to multiple states of resistance (as disclosed in co. 8, lines 4-10, and col. 12, lines 6-44; forming a second conductive line 42, the second conductive line 42 in electrical communication with one of the memory cells 30; and creating a third conductive line 29 in electrical communication with the first conductive line 12 and the plurality of memory cells 30, wherein the memory cells comprise an element having an alterable resistance for the disclosed intended purpose of forming

directly overwritable, electronic, non-volatile, high-density, low cost memory cells that exhibit orders of magnitude higher switching speeds at remarkably reduced energy levels, due to the chalcogenide materials, as disclosed in col. 5, lines 14-28.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the memory cell comprising an element programmable to multiple states of resistance, wherein the element is formed as part of the memory cell for the disclosed intended purpose of forming directly overwritable, electronic, non-volatile, high-density, low cost memory cells that exhibit orders of magnitude higher switching speeds at remarkably reduced energy levels, due to the chalcogenide materials, as disclosed in col. 5, lines 14-28.

Becker as modified by Ovshinsky above, discloses the claimed invention with the exception of forming a plurality of first conductive lines disposed with one of the first conductive lines overlying and in electrical communication with a selected one of the memory cells.

Gonzalez et al. discloses in Fig. 15 and in cols. 5 to 9, a method of making a memory array, that includes forming a contact plug 175 in an insulating layer 40 wherein the memory cells are formed, forming a plurality of first conductive lines 130 disposed with one of the first conductive lines overlying and in electrical communication with a selected one of the memory cells; and forming a second conductive line 190 in a second conductive layer, the second conductive line 190 in electrical communication with the contact plug 175, wherein a plurality of first

conductive lines are disposed with one of the first conductive lines overlying an in electrical communication with a selected one of the memory cells for the disclosed intended purpose of providing electrical interconnection between the memory cells of the cell array as disclosed in col. 8, lines 34-45 of Gonzalez et al..

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a conductive line overlying an in electrical communication with a selected one of the memory cells for the disclosed intended purpose of providing electrical interconnection between the memory cells of the cell array as disclosed in col. 8, lines 34-45 of Gonzalez et al...

Regarding claim 48, Becker discloses forming a plurality of contact plugs 54 between the digit line 28 and the second conductive line 56, a respective one of the plurality of contact plugs being formed between respective pairs of memory cells.

Regarding claim 53, Becker as modified by Ovshinsky discloses forming each of the memory cells to have a width approximately equal to a minimum photolithographic limit as disclosed by Ovshinsky in col. 12,lines 36-44.

Regarding claim 54, Becker as modified by Ovshinsky discloses in col. 14, lines 13-20 that the forming of the memory cells, each pair being spaced apart by a distance that is limited only by the resolution of the lithography.

Regarding claim 55, Becker, as modified by Ovshinsky in col. 11, lines 47-53 discloses that each contact 14 may be formed from a doped semiconductive region of the substrate.

Regarding claim 56, Becker as modified by Ovshinsky discloses that the step of forming a plurality of contacts comprises forming dielectric spacers 16 between each pair of memory cells; and forming each contact 14 between the respective dielectric spacers 16.

Regarding claim 57, Becker as modified by Ovshinsky discloses in col. 14, lines 13-20 that the forming of the structure, including each contact and its respective dielectric spacers have a combined width that is limited only by the resolution of the lithography.

Regarding claim 58, Becker discloses isolating each of the plurality of memory cells from the plurality of contacts 54.

Regarding claim 59, Becker discloses that isolating comprises disposing dielectric material 52 on each of the plurality of memory cells.

Regarding the limitation that the method comprises forming each of the memory cells to have a width approximately equal to a minimum photolithographic limit and being spaced apart by a distance approximately equal to the minimum photolithographic limit, it would have been an obvious matter of design choice to form the memory cells having a width approximately equal to a minimum photolithographic limit, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955). Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made

to change the size of the feature as there is no statement denoting the criticality of the width of the memory cells beyond the knowledge of one of ordinary skill in the art of reducing the semiconductor features' sizes.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

6. Claims 36, 46, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinsky as applied to claims 19, 35, and 40-45 above, and further in view of Ikeda et al..

Ovshinsky as applied above discloses the claimed invention with the exception of disposing dielectric material on each of the plurality of memory cells in order to isolate the memory cells from the contacts.

Ikeda et al. discloses in figs. 9, and 26-32, a method for making a memory device that comprises providing a substrate having a first conductive line 13 therein; forming a plurality of memory cells; forming a second conductive line 29, the second conductive line 29 in electrical communication with one of the memory cells; and creating a third conductive line 33 in electrical communication with the first conductive line and the plurality of memory cells, wherein the third conductive line 33 is created for the well known and disclosed intended purpose of connecting the memory cells to other areas of the circuit; forming a plurality of contacts between the first conductive line 13 and the

third conductive line 33, a respective one of the plurality of contacts being formed between respective pairs of memory cells, and forming each contact from a doped semiconductive region of the substrate; disposing dielectric material on each of the plurality of memory cells; and forming a first titanium silicide layer over the first conductive line; wherein the plurality of contact are isolated from the memory cells by disposing dielectric material on each of the plurality of memory cells for the disclosed intended purpose of providing electrical communication between the digit line and other areas of the circuit while being isolated from the memory cells.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the plurality of contact be isolated from the memory cells by disposing dielectric material on each of the plurality of memory cells for the disclosed intended purpose of providing electrical communication between the digit line and other areas of the circuit while being isolated from the memory cells.

Ovshinsky as modified by Ikeda et al. further discloses forming a titanium silicide layer over the first conductive line.

7. Claims 49 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Becker (U. S. Pat. 5,770,498) in view of Ovshinsky (U. S. Pat. 5,296,716) and Gonzalez et al. (U. S. Pat. 5,150,276) as applied to claims 20, 48, and 53-59 above, and further in view of Ikeda et al..

Becker as modified by Ovshinsky and Gonzalez et al. above discloses the claimed invention with the exception of forming a titanium silicide layer over the digit line, and

forming the second conductive line through tapered holes extending through the dielectric material to the contact plugs.

Ikeda et al. discloses in figs. 9, and 26-32, a method for making a memory device that comprises providing a substrate having a first conductive line 13 therein; forming a plurality of memory cells; forming a second conductive line 29, the second conductive line 29 in electrical communication with one of the memory cells; and creating a third conductive line 33 in electrical communication with the first conductive line and the plurality of memory cells, wherein the third conductive line 33 is created for the well known and disclosed intended purpose of connecting the memory cells to other areas of the circuit; forming a first titanium silicide layer over the first conductive line; forming dielectric spacers 15 between each pair of memory cells and forming each contact between the respective dielectric spacers, and forming the conductive line through tapered holes extending through the dielectric material to the contacts; wherein a first titanium silicide is formed over the conductive line for the disclosed intended purpose of reducing the resistance of the contact region so that it can accelerate the signal transmission rate, and forming the conductive line through tapered holes for the well known purpose of aiding in the filling of the contact plugs.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a titanium silicide film over the conductive line for the disclosed intended purpose of reducing the resistance of the contact region so that it can accelerate the signal transmission rate, and forming the conductive line through tapered

holes for the well known purpose of aiding in the filling of the contact plugs, as Ikeda et al. teaches.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571) 272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GP

ANH D. MAI
PRIMARY EXAMINER